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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) : Martin VORBACH et al.

Serial No : 09/145,139

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For : INTERNAL BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES, FOR MANAGING LARGE VOLUMES OF DATA WITH A HIGH INTERCONNECTION COMPLEXITY

Group Art Unit : 2781

Examiner : T. Vo

Assistant Commissioner
for Patents
Washington, D.C. 20231

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Date: 2/12/01 Reg. No. 41,172

Signature: _____
Dervis Magistre

AMENDMENT

SIR:

This paper addresses the Office Action dated August 11, 2000. Initially, kindly amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

22. (Twice Amended) The method according to claim 18 [19], wherein the module having the multi-dimensional cell architecture includes at least one of a field programmable gate array and a dynamically configurable gate array.

23. (Twice Amended) The method according to claim 18 [19], wherein the module having the multi-dimensional cell architecture includes a module having a two-dimensional programmable cell architecture.